argon; fluorine; nitrogen; III b-element; IV b-element; V b-element; VI b-element; VII b-element; IV a-element; and V a-element.

a3

17. (Newly Added) A semiconductor device as recited in claim 12, wherein said fuse element is a laser blown fuse element.

18. (Newly Added) A semiconductor device as recited in claim 14, wherein said fuse element is a laser blown fuse element.

REMARKS

Applicant gratefully recognizes acknowledgement of claim for foreign priority under 35 U.S.C. §119, as well as receipt of the certified copies of the priority documents.

The above Amendment to the specification is being submitted to correct errors noticed in review of the specification during preparation of the present Amendment. These corrections are believed, in good faith, to clarify the disclosure, while adding no new matter.

Reconsideration and allowance of all claims of records are respectfully requested. Claims 10 – 18 are pending upon entry of the present Amendment. Claims 15 – 18 have been added by this Amendment. Claims 10 and 13 are independent claims.

Brief Synopsis of the Illustrative Embodiments

The present invention as described in connection with the exemplary embodiments in the present application is drawn to a semiconductor device and its method of manufacture, which substantially overcomes one or more of the problems due to limitations and disadvantages of the related art.

According to one exemplary embodiment of the present invention shown in Fig. 3(a), a dummy layer 34 of a predetermined shape is formed on a first insulating layer 33. A spin-on-glass (SOG) layer 35 is above the dummy layer 34. The surface of the SOG layer 35 is converted by ion implantation to a dense layer 35b. As a result, as is illustrated in Fig. 3(b), the SOG layer 35 is converted to a laminated structure which is composed of the surface layer 35b and a base layer 35a, wherein the surface layer 35b is

relatively more dense than the base layer 35a. (See for example pg. 14, lines 20-27 of the application as filed).

A second insulating layer 37 is disposed on the second SOG layer 35b. The first and second insulating layers and the first and second SOG layers are exposed at a boundary between the first region and the second region. Illustratively, the boundary corresponds to the side surface of the opening 39 as shown in Fig. 3(c).

Rejection Over Morozumi, et al. in View of La Fleur, et al. Under 35 U.S.C.§103(a)

Claims 10 – 14 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Morozumi, et al.* (U.S. 6,246,105) in view of *La Fleur, et al.* (U.S. 5,903,041).

The establishment of a *prima facie* case of obviousness under 35 U.S.C.§103(a) requires that *all* of the elements be found in the prior art. It follows, therefore, that if a **single** claimed element **is not found** in the applied prior art, a *prima facie* case of obviousness cannot be established. Moreover, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is a teaching, suggestion or motivation to do so found in the references relied upon wherein the knowledge generally available to one having ordinary skill in the art. However, hindsight is never an appropriate motivation for combining references and/or the knowledge generally available to one having ordinary skill in the art. To this end, relying upon hindsight knowledge of Applicants' disclosure when the prior art does not teach nor suggest such knowledge results in the use of the invention as a template for its own reconstruction. This is wholly inappropriate in the determination of patentability.

For at least the following reasons, it is respectfully submitted that the Office Action has failed to establish a *prima facie* case of obviousness because at least the presently discussed claimed elements are not found in the applied prior art.

The reference to *Morozumi, et al.* is drawn to a semiconductor device and process of manufacturer having a protective insulation film, which affords certain advantages. The Office Action asserts that a first SiO_2 is formed on the side surface of the dummy pattern 37 and the first insulating layer 12. The Office Action then states that the reference to *Morozumi, et al.* does not teach the method of forming of this oxide layer (first SiO_2 layer 20), but does disclose spin-on-glass (SOG) as an acceptable method of

forming this layer. For the reasons that follow, Applicants respectfully disagree with the assertions of the Office Action described immediately above.

First, in the reference to *Morozumi, et al.*, reference numeral 37 refers to a wiring layer, which is comprised of a polysilicon film and a tungsten silicide film formed on the field insulation film (FOX) 12. As such, it is respectfully submitted that *Morozumi, et al.* does not teach the dummy layer as set forth in claims 10 and 13, and which illustratively prevents moisture from being introduced into an internal circuit of the semiconductor device (See pg. 14, lines 5-9 of the application as filed, for example). (Please refer to Fig. 1 of *Morozumi, et al.* as well as column 6, lines 22-26).

Secondly, the reference to *Morozumi, et al.* clearly states that the first silicon oxide film 20 (SiO_2 layer 20) is formed by the reaction between tetraetoxysilane (TEOS) and oxygen by a plasma chemical vapor deposition. (See column 7, lines 1-5 of the reference to *Morozumi, et al.*). It is submitted that the TEOS reaction results in the formation of SiO_2, which is not the same material as SOG which is specifically claimed in independent claims 10 and 13. To this end, the oxidation reaction of TEOS results in the formation of silicon dioxide, a process which is well-known in the semiconductor fabrication arts. In contrast, SOG materials of the present invention are formed by dissolving a silicon compound in an organic solvent to obtain a SOG solution, which is applied and baked. Upon heat treatment the SOG materials become SiO_2-like in character, and can be used instead of SiO_2 as interlayer dielectrics. Accordingly, the first SOG layer as recited in independent claims 10 and 13 is not the same material as the first SiO_2 layer 20 as is asserted in the Office Action. (Applicants provide herewith in a Supplemental IDS pertinent portions of a textbook by Ghandi which discusses TEOS-SIO_2 and spin-on-glass. From a review of these portions, a reasonable inference may be drawn that SOG and TEOS-SIO_2 are not the same material).

Third, protective insulation films as discussed in the description of the related art in the reference to *Morozumi, et al.* does disclose the use of a spin-on-glass (SOG) film and a silicon nitrite film formed by plasma chemical vapor deposition. However, there is no teaching nor suggestion that such a film would be used for the first SiO_2 layer 20 of the reference to *Morozumi, et al.* As noted above, the first SiO_2 layer 20 is fabricated by a TEOS reaction. Moreover, because the reference to SOG films is contained within the

Description of the Related Art of *Morozumi, et al.*, a reasonable inference could be drawn that the reference to *Morozumi, et al.* in fact considers these materials to be undesirable. While in no way agreeing that the use of SOG is undesirable, it is respectfully asserted that the reference to *Morozumi, et al.* may in fact teach a way from the use of SOG, and therefore, could not be properly applied to the pending claims of the present application.

The Office Action further asserts that first and second insulating layers, and first and second spin-on-glass (SOG) layers are exposed at a boundary between the first region and the second region. (The Office Action at pg. 3 refers to Fig. 5 of the reference to *Morozumi, et al.* in this portion of the Rejection). Applicants respectfully disagree with this assertion. To this end, in accordance with an exemplary embodiment of the present invention shown in Fig. 3(c), the boundary as recited in claims 10 and 13 between the first region and the second region corresponds to the side surface of opening 39. A review of Fig. 5 of *Morozumi, et al.* reveals no teaching nor suggestion of this feature. In fact, a review of Fig. 5 of *Morozumi, et al.* shows no such exposure at a boundary between first and second regions. Accordingly, because at least the presently described claim limitation of claims 10 and 13 is neither taught nor suggested in the reference to *Morozumi, et al.*, the reference to *Morozumi, et al.* cannot serve to establish a *prima facie* case of obviousness.

For at least the reasons set forth above, it is respectfully submitted that the reference to *Morozumi, et al.* lacks at least the elements of claims 10 and 13 discussed above. As such, the rejection of claims 10 and 13, and the claims that depend therefrom, in view of *Morozumi, et al.* alone or in combination with the applied art is believed to be improper. Withdrawal of the rejection of claims 10 and 13, and the claims that depend therefrom is respectfully requested, and the allowance thereof is earnestly solicited.

Newly Added Claims

Claims 15 – 18 have been added to further recite details of the present invention in accordance with independent claims 10 and 13. These claims are believed to be allowable for at least the reasons that claims 10 and 13 are believed to allowable. Allowance of these newly added claims is respectfully requested.

CONCLUSION

In view of the foregoing amendments and remarks, reconsideration and withdrawal of all objections and rejections of pending claims 10 - 18 are respectfully requested. An early notice of allowance is earnestly solicited.

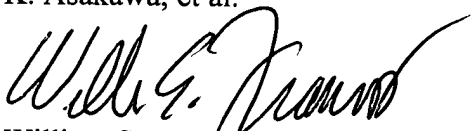
Except as otherwise stated in the previous Remarks, applicants note that each of the amendments have been made to place claims in better form for U.S. practice or to clarify the meaning of the claims; and not to distinguish the claims from prior art references, otherwise narrow the scope, or comply with other statutory requirements.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact William S. Francos, Esq. (Reg. No. 38,456) at (610) 375-3513 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies to charge payment or credit any overpayment to Deposit Account Number 50-0238 for any additional fees under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17.

Respectfully submitted on behalf of:

K. Asakawa, et al.



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Enclosures: (1.) Marked-Up Version of Amended Paragraphs Showing Changes

Marked-Up Version of Amended Paragraphs Showing Changes:

The SOG film 18 having the laminated structure (18a and 18b) which is the same as that of the first preferred embodiment is formed over the gate electrodes 14 so as to cover the gate electrodes 14. The conductive part [12] 21 as a bit line is formed between the gate electrodes 14. The conductive part [12] 21 is the same as that of the first preferred embodiment. The two memory cells share conductive part [12] 21. The conductive part 21 as the bit line can be formed in the same manner as explained in Fig. 1(a) through Fig. 1(c).

When the SOG film 35 having the relatively high moisture absorption property exists between the top surface of the dummy layer 34 and the insulator 37, [such] the SOG film 35 may act as a path through which the moisture passes. In the conventional technique, [such] the SOG film 35 located between the top surface of the dummy layer 34 and the insulator 37 is removed by etching back the entire surface of the SOG film 35 to overcome the moisture passing problem. Then, the insulator 37 and the cover film 38 are formed over the etched surface of the SOG film 35.